NASA TECH BRIEF

Complementary-MOS Binary Counter With Parallel-Set Inputs

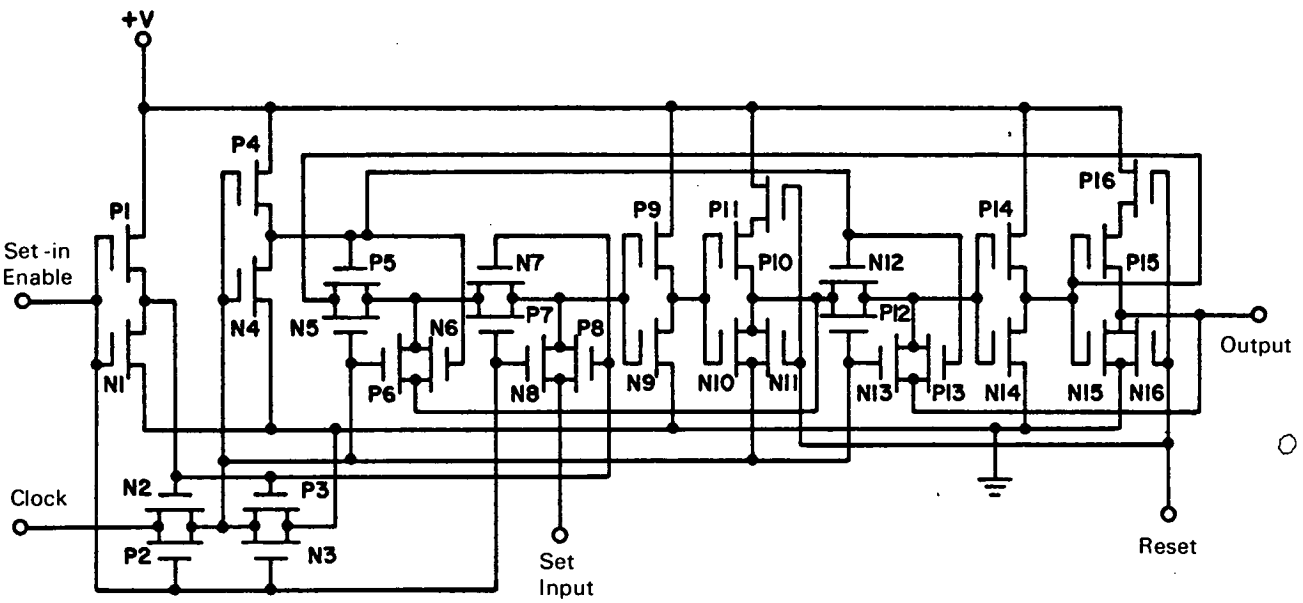

Figure 1. Basic Counter Circuit

The problem:

To design a complementary metal-oxide semiconductor (MOS) four-stage binary counter containing reset capability as well as four parallel-set inputs gated in by a logic signal.

The solution:

A basic counter stage similar to a counter circuit described by A. Rapp (1967 ISSCC Digest, pp. 52-53). The modified circuit features a new reset scheme plus four parallel-set inputs gated in by the "set-in enable" signal. Four parallel-set inputs permit setting the counter into any of sixteen possible states.

Figure 1 shows a basic counter stage using a D-T flip-flop consisting of two cross-coupled flip-flops. This counter, an upcounter, changes state on the negative-going edge of the clock signal. The "set-in enable" signal gates in the set-input information. With the "set-in enable" at +V, the internal clock line (i.e., gates of P4 and N4) assumes ground potential because transmission gate P3-N3 is on. Transmission gate P7-N7 opens, unlocking the first flip-flop and allowing the set-input signal to transfer into the first flip-flop through transmission gate P8-N8, and then through transmission gate P12-N12 to the output. When the "set-in enable" signal returns to ground, the first or second flip-flop (depending upon whether the clock signal is at ground or +V potential) will be locked and a state change will not occur at the counter state output. This counter circuit main-

(continued overleaf)

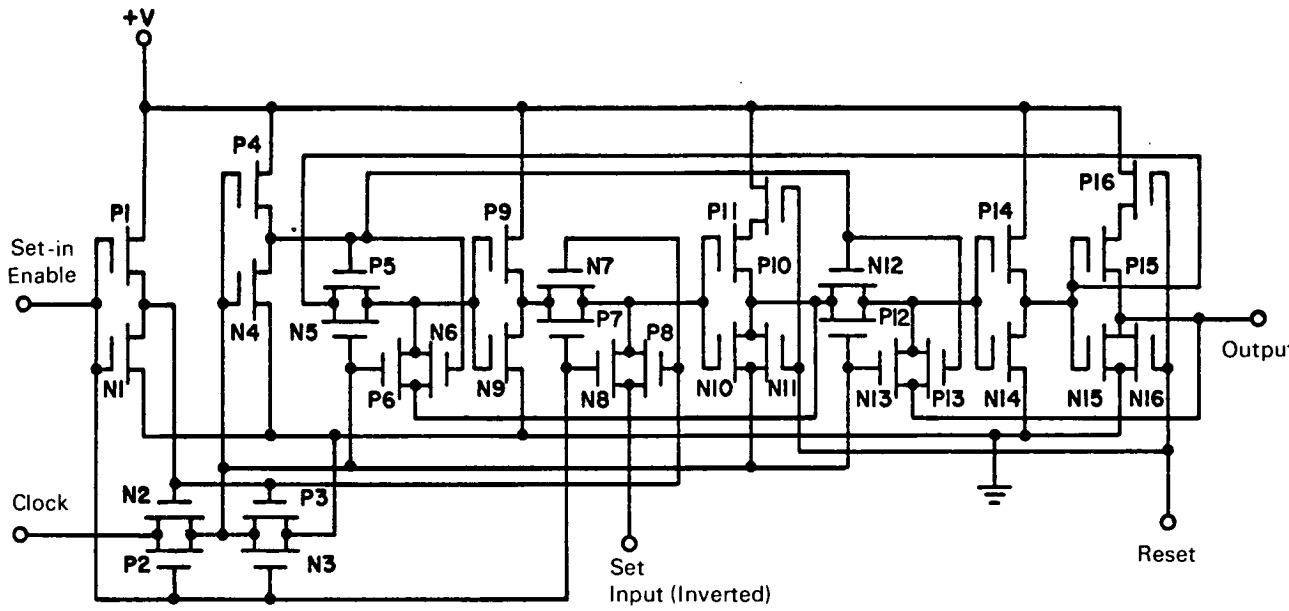

Figure 2. Alternate Version of Counter Circuit

tains its set state after the "set-in enable" signal returns to ground, independent of the potential at the clock input.

Figure 2 shows an alternate version of the counter stage with a modified set-input gating circuit. Instead of placing transmission gates P7-N7 and P8-N8 at the input of inverter P9-N9, they are placed at the inverter output. This configuration eliminates the two series transmission gates, P5-N5 and P7-N7 in Figure 1. Two series transmission gates invariably slow the circuit operation. Isolating the two transmission gates with an inverter driver improves operational speed. An inverted set-input signal is required to set the counter stage because inversion takes place from the set-input to the stage output.

Notes:

1. A breadboard counter has been operated at clock rates to 5 MHz.
2. This circuit should be useful in computer applications as a special purpose counter with parallel-gated inputs and simple data-hold capability.
3. The following documentation may be obtained from:

   Clearinghouse for Federal Scientific and Technical Information
   Springfield, Virginia 22151
   Single document price $3.00
   (or microfiche $0.65)

   Reference:
   NASA-CR-86171 (N69-30472), Design and Development of a Digital Subsystem Employing N- and P- Channel MOSFET's in Complementary Circuits in An Integrated Circuit Array

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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